a transistor gate over said substrate and wholly between said spaced doped source/drain regions, said transistor gate having one first gate electrode of a first conductivity type and two second gate electrodes of a second conductivity type, wherein said two second gate electrodes are provided on either side of said first gate electrode and are separated from said first gate electrode by an insulating dielectric layer.

33. (Amended) A semiconductor device, comprising:

a semiconductor substrate, said substrate having at least two separated doped source/drain regions;

three gate electrodes over said substrate and at least partially between said source/drain regions, including a center gate electrode of P+ type conductivity and two adjacent outer gate electrodes of N+ type conductivity;

a gate dielectric separating said three gate electrodes from said substrate;

a thin dielectric layer separating said outer gate electrodes from said center gate electrode;

a first conductive cap layer over said center gate electrode and a second conductive cap layer electrically connecting said outer gate electrodes; and

insulating sidewalls adjacent to said conductive cap layer and said outer gate electrodes.

34. (Amended) The semiconductor device of claim 33, wherein the three gate electrodes comprise doped polysilicon.

35. (Amended) The semiconductor device of claim 33, wherein the center gate electrode comprises silicon-germanium.

36. (Amended) The semiconductor device of claim 33, wherein the three gate electrodes comprise a material selected from the group consisting of silicon-carbide and silicon oxycarbide.

Q2

37. (Amended) The semiconductor device of claim 33, wherein the dielectric layer comprises a material selected from the group consisting of nitride, oxynitride, and nitrided oxide.

40. (Amended) The semiconductor device of claim 33, wherein a workfunction difference exists between the center gate electrode and the outer gate electrodes.

41. (Amended) The semiconductor device of claim 40, wherein said workfunction difference results in the center gate electrode having a higher threshold voltage than said outer gate electrodes.

G3

42. (Amended) A transistor structure comprising:

a semiconductor substrate having at least two spaced doped source/drain regions, said source/drain regions defining a channel region therebetween;

a gate dielectric over said substrate;

a central gate electrode over said channel region and said gate dielectric; and

two outer gate electrodes over said channel region and said gate dielectric and adjacent to said central gate electrode, said outer gate electrodes being separated from said central gate electrode by a dielectric layer, and wherein said gate dielectric where under said two outer gate electrodes is equal in thickness to or thinner than said gate dielectric where under said central gate electrode;

Q3 wherein a workfunction difference between the central gate electrode and the outer gate electrodes is such that said central gate electrode experiences a greater threshold voltage than said outer gate electrodes.